WHAT IS CLAIMED IS:

1. A resampler for use with a bit pump having a receive path couplable to an oscillator, comprising:

an interpolation stage, coupled to an input of said resampler, configured to receive a one-bit input signal representing at least a portion of a receive signal propagating along said receive path and generate a plurality of intermediate samples from at least two input samples associated with said one-bit input signal; and

a selection stage, coupled to said interpolation stage, configured to select one of said plurality of intermediate samples thereby providing an output sample that corresponds to a phase of said oscillator.

2. The resampler as recited in Claim 1 wherein said interpolation stage is configured to receive multiple one-bit input signals representing at least a portion of said receive signal and generate a corresponding plurality of intermediate samples from at least two input samples associated with each of said multiple one-bit input signals.

3. The resampler as recited in Claim 2 wherein said selection stage is configured to select corresponding ones of said plurality of intermediate samples thereby providing output samples that correspond to said phase of said oscillator.

4. The resampler as recited in Claim 3 further comprising a combining stage configured to combine said output samples.

5. The resampler as recited in Claim 1 further comprising a filter stage configured to filter said output sample.

6. The resampler as recited in Claim 5 wherein said filter stage comprises one of a second and third order section.

7. The resampler as recited in Claim 1 further comprising a delay stage.

8. A method of resampling at least a portion of a receive signal propagating along a receive path couplable to an oscillator of a bit pump, comprising:

receiving a one-bit input signal representing said at least a portion of said receive signal;

generating a plurality of intermediate samples from at least two input samples associated with said one-bit input signal; and

selecting one of said plurality of intermediate samples thereby providing an output sample that corresponds to a phase of said oscillator.

9. The method as recited in Claim 8 further comprising receiving multiple one-bit input signals representing at least a portion of said receive signal and generating a corresponding plurality of intermediate samples from at least two input samples associated with each of said multiple one-bit input signals.

10. The method as recited in Claim 9 further comprising selecting corresponding ones of said plurality of intermediate samples thereby providing output samples that correspond to said phase of said oscillator.

11. The method as recited in Claim 10 further comprising combining said output samples.

12. The method as recited in Claim 8 further comprising filtering said output sample.

13. The method as recited in Claim 12 wherein said filtering is performed by a filter stage having one of a second and third order section.

14. The method as recited in Claim 9 further comprising delaying ones of said multiple one-bit input signals.

15. A bit pump having a transmit and receive path, comprising:

a precoder, coupled to said transmit path, that preconditions a transmit signal propagating along said transmit path;

a modulator, coupled to said precoder, that reduces a noise associated with said transmit signal;

an analog-to-digital converter, coupled to said receive path, that converts a receive signal received at said bit pump into a digital format;

a resampler, coupled to said analog-to-digital converter and an oscillator of said bit pump, including:

an interpolation stage, coupled to an input of said resampler, that receives a one-bit input signal representing at least a portion of said receive signal and generates a plurality of intermediate samples from at least two input samples associated with said one-bit input signal, and

a selection stage, coupled to said interpolation stage, that selects one of said plurality of intermediate samples thereby providing an output sample that corresponds to a phase of said oscillator; and

an echo canceling system, coupled between said transmit and receive path, that attenuates an echo in said receive signal.

16. The bit pump as recited in Claim 15 wherein said interpolation stage receives multiple one-bit input signals representing at least a portion of said receive signal and generates a corresponding plurality of intermediate samples from at least two input samples associated with each of said multiple one-bit input signals.

17. The bit pump as recited in Claim 16 wherein said selection stage selects corresponding ones of said plurality of intermediate samples thereby providing output samples that correspond to said phase of said oscillator.

18. The bit pump as recited in Claim 17 wherein said resampler further comprises a combining stage that combines said output samples.

19. The bit pump as recited in Claim 15 wherein said resampler further comprises a filter stage that filters said output sample.

20. The bit pump as recited in Claim 19 wherein said filter stage comprises one of a second and third order section.

21. The bit pump as recited in Claim 15 wherein said resampler further comprises a delay stage.

22. A transceiver, comprising:

a framer that formats signals within said transceiver;

a bit pump coupled to said framer and having a transmit and receive path, including:

a precoder, coupled to said transmit path, that preconditions a transmit signal propagating along said transmit path;

a modulator, coupled to said precoder, that reduces a noise associated with said transmit signal;

an analog-to-digital converter, coupled to said receive path, that converts a receive signal received at said bit pump into a digital format;

a resampler, coupled to said analog-to-digital converter and an oscillator of said bit pump, including:

an interpolation stage, coupled to an input of said resampler, that receives a one-bit input signal representing at least a portion of said receive signal and generates a plurality of intermediate samples from at least two input samples associated with said one-bit input signal, and

a selection stage, coupled to said interpolation stage, that selects one of said plurality of intermediate

samples thereby providing an output sample that corresponds to a phase of said oscillator; and

an echo canceling system, coupled between said transmit and receive path, that attenuates an echo in said receive signal; and

a controller that controls an operation of said framer and said bit pump.

23. The transceiver as recited in Claim 22 wherein said interpolation stage receives multiple one-bit input signals representing at least a portion of said receive signal and generates a corresponding plurality of intermediate samples from at least two input samples associated with each of said multiple one-bit input signals.

24. The transceiver as recited in Claim 23 wherein said selection stage selects corresponding ones of said plurality of intermediate samples thereby providing output samples that correspond to said phase of said oscillator.

25. The transceiver as recited in Claim 24 wherein said resampler further comprises a combining stage that combines said output samples.

26. The transceiver as recited in Claim 22 wherein said resampler further comprises a filter stage that filters said output sample.

27. The transceiver as recited in Claim 26 wherein said filter stage comprises one of a second and third order section.

28. The transceiver as recited in Claim 21 wherein said resampler further comprises a delay stage.